



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/450,054

11/29/1999

ASHOK V. KRISHNAMOORTHY

32

7078

26291

7590

02/18/2004

MOSER, PATTERSON & SHERIDAN L.L.P.
595 SHREWSBURY AVE
FIRST FLOOR
SHREWSBURY, NJ 07702

EXAMINER

JACKSON, CORNELIUS H

ART UNIT

PAPER NUMBER

2828

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/450,054	Applicant(s) KRISHNAMOORTHY, ASHOK V.	
	Examiner Cornelius H. Jackson	Art Unit 2828	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 15 January 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) ☐ they raise the issue of new matter (see Note below);
 - (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☐ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: 1-11.

Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Paul J.
SPE 2828

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4-5 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Koh et al. (5416861). Koh et al. disclose a network **Fig. 1** for distributing a power signal in an optoelectronic circuit **20** comprising a plurality of electrically conductive pathways, **see col. 3, line 3-col. 4, line 14** forming at least a first level, wherein each level is comprised of a plurality of segments **24** linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level; means for coupling **16, 18 and 22** the power signal from a primary input to the common point of the first level; terminal nodes **26** coupled at the extremities of a last level for supplying the power signal to a plurality of devices that form at least a portion of said optoelectronic circuit **20**, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

Regarding claims 2, Koh et al. disclose all stated limitations, **see Figs. 1-2**.

Regarding claim 4, Koh et al. disclose a network on an optoelectronic chip, **see col. 1, lines 48-54 and col. 26, lines 13-14.**

Regarding claim 5, Koh et al. disclose the terminal nodes are optoelectronic devices, **see claim 18.**

Regarding claims 10-11, it is inherent that the device claimed operates on using method claimed, therefore the rejection of the device applies also for the method.
(Also, see col. 10, lines 31-56.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh et al. (5416861) in view of Watanabe (5309001). Kohl et al., as applied to claims 1 and 2 above, teach all of the stated limitations except for that the pattern of the level is X-shaped. Watanabe et al. teach the levels form an X-shaped pattern, **see Figs. 5, 10, 16 and 18a.** Since it has been held to be within the general skill of a worker in the art to select a known design on the basis of its suitability for the intended use as a matter of obvious design choice. Also, it would have been an obvious matter of design choice to change the shape of the pattern used to equally distribute the power signal,

Art Unit: 2828

since applicant has not disclosed that pattern shape solves any stated problem or is for any particular purpose and it appears that the prior art would perform equally well with the H-shaped pattern.

Regarding claim 6, Watanabe et al. teach the terminal node maybe a VCSEL. Also, it is well known that VCSELs are a form of integrated circuits, therefore it would only be a matter of design choice. Since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 7 and 9, see claims 1 and 3 above.

Regarding claim 8, see claims 1-3 above.

5. Claims 1-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5309001). Watanabe et al. teach a network **Fig. 12a** for distributing a power signal in an optoelectronic circuit **350** comprising a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments **353a-358b** linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level; means for coupling **347/352** the power signal from a primary input to the common point of the first level; terminal nodes **359a-b** coupled at the extremities of a last level for supplying the power signal to a device that form at least a portion of said optoelectronic circuit **350**, wherein the number

Art Unit: 2828

of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal, **see col. 9, line 13-col. 26, line 20**. Watanabe et al. fail to teach the power signal is supplied to a plurality of devices; instead, Watanabe et al. teach the power signal is supplied to a plurality of portions of a single device. It would have been obvious to one of ordinary skill in the art at the time the invention was made divide the device into multiple sections, since it is inherent that each portion of the single device of Watanabe would operate as an individual unit having its own power signal. Also, the fact that Watanabe uses the network on a single device, instead of a plurality of devices does not negate the fact that both networks are the same/identical invention and the structure of Watanabe is capable of performing the intended use of distributing a power signal to a plurality of devices; therefore, Watanabe meets the claim. Since it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 2, Watanabe et al. teach all stated limitations, **see Figs. 12a.**

Regarding claim 3, Watanabe et al. teach all stated limitations, **see Figs. 16.**

Regarding claim 4, Watanabe et al. teach all stated limitations, **see col. 15, lines 49-51 and claim 1 above.**

Regarding claim 5, Watanabe et al. teach the terminal nodes are optoelectronic devices, **see col. 15, line 43-51 and claim 1 above.**

Regarding claims 10-11, it is inherent that the device claimed operates, using method as claimed; therefore, the rejection of the device applies to the method as well.

6. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (5309001) in view of Olbright et al. (5266794)/Schneider et al. (5351256)/Lebby et al. (5337397). Watanabe et al., as applied to claims 1-5 above, teach all of the stated limitations except for the integrated circuits are VCSELs; instead, Watanabe et al. teach the integrated circuits are LEDs. It is well known in the laser art that one may use either laser source (e.g. LED or VCSEL) as a matter of obvious design choice, **see Olbright et al. col. 8, lines 65-68/Schneider et al. col. 1, lines 14-16/ Lebby et al. col. 3, lines 17-27.** Since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 7-9, Watanabe et al. teach all the stated limitations except for the plurality of electrically conductive pathways being separate; instead, Watanabe et al. teach the pathways being formed of wider/broader pathways that diverge as it branches to a higher level/order, **see Figs. 5, 7, 9-10 and 18a and col. 9, line 54-col. 10, line 3, col. 11, line 11-col. 13, line 47 and col. 24, line 33-col. 26, line 20.** It would have been an obvious to one having ordinary skill in the art at the time the invention was

Art Unit: 2828

made to separate the diverging wider/broader pathways into the individual pathways the wider/broader pathways eventually become, since the examiner takes Office Notice of the equivalence of the diverging wider/broader pathways and the plurality of separate pathways for their use in the electrical art and the selection of any of these known equivalents to improve the flow of current from a primary source to multiple regions would be within the level of ordinary skill in the art.

Response to Arguments

7. Applicant's arguments filed 15 January 2004 have been fully considered but they are not persuasive, since the claimed device has no structural difference than the device of the stated prior art. Applicant argued the following:

a. "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" and Koh discloses an optical waveguide H-tree design, instead of an electrically conductive pathway.

b. Koh discloses an H-tree configuration for equidistant clock distribution, not power distribution.

c. Koh fails to disclose "wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths".

In response to Applicant arguments:

a. Koh discloses each and every element of the claimed invention, arranged as
~~in the claim, since Koh teaches that the optical pathways maybe superconductor~~
pathways, **see col. 1, line 67** and Koh also teaches the electrical H-tree clock
distribution to be well known, **see col. 3, lines 3-7**.

b. Both electrical and optical signals are power signals, although the power
signals maybe used for carrying information and/or other task. Also, a recitation of the
intended use of the claimed invention must result in a structural difference between the
claimed invention and the prior art in order to patentably distinguish the claimed
invention from the prior art. If the prior art structure is capable of performing the
intended use, then it meets the claim. In a claim drawn to a process of making, the
intended use must result in a manipulative difference as compared to the prior art. See
In re Casey, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA
1963).

c. Koh discloses "wherein each level is comprised of a plurality of segments
linearly extending from a common point, each of the segments of respective levels
having equal lengths", **see Figs. 1 and 2**.

Conclusion

Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Cornelius H. Jackson whose telephone number is

Art Unit: 2828

(571)272-1942. The examiner can normally be reached on 8:00 - 5:00, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Ip can be reached on (571)272-1941. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



chj

Response
Serial No. 09/450,054
Page 2

Amendments to the Claims

Please amend claims 1 and 7 as follows:

1. (Currently Amended) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to [a] the common point at the center of the first level; and

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

2. (Previously Presented) The network of claim 1 wherein each level is at least one H-shaped pattern comprising first and second parallel branches each having a respective first and second midpoint, and a third branch interconnecting said first and second midpoints, and wherein said center of said H-shaped pattern is the midpoint of said third branch.

3. (Previously Presented) The network of claim 1 wherein each level is at least one X-shaped pattern comprising first and second branches each having a respective first and second midpoint and interconnecting said first and second

Response
Serial No. 09/450,054
Page 3

branches at said midpoints, and wherein said center of said X-shaped pattern is the intersection of said first and second branches.

4. (Previously Presented) The network of claim 1 wherein said network is located on an optoelectronic chip.

5. (Previously Presented) The network of claim 1 wherein said terminal nodes are optoelectronic devices.

6. (Previously Presented) The network of claim 1 wherein said terminal nodes are VCSELS

7. (Currently Amended) A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of separate electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths and wherein said pathways are joined only at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point;

means for coupling said power signal from a primary input to [a] the common point at the center of the first level;

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal.

8. (Previously Presented) The network of claim 7 wherein each level is at

Response
Serial No. 09/450,054
Page 4

least one H-shaped pattern comprising first and second parallel branches each having a respective first and second midpoint, and a third branch interconnecting said first and second midpoints, and wherein said center of said H-shaped pattern is the midpoint of said third branch.

9. (Previously Presented) The network of claim 7 wherein each level is at least one X-shaped pattern comprising first and second branches each having a respective first and second midpoint and interconnecting said first and second branches at said midpoints, and wherein said center of said X-shaped pattern is the intersection of said first and second branches.

10. (Previously Presented) A method of distributing a power signal to a plurality of terminal nodes on an optoelectronic circuit, the method comprising the steps of:

receiving the power signal from a primary input; and

directing said power signal to said plurality of terminal nodes using an H-tree network, said H-tree network including at least a first level, wherein the first level is coupled to said primary input, and a last level includes said plurality of terminal nodes for supplying said power signal to a plurality of devices, each of said at least one level having a plurality of segments, each segment of a respective plurality is equal in length; and

wherein a number of segments from said primary input to each of said terminal nodes is equal such that the power supplied by each of the terminal nodes to each of the plurality of devices is substantially equal.

11. (Previously Presented) The method of claim 10, wherein the directing step further includes directing said power signal to said plurality of terminal nodes using an H-tree network,

wherein said plurality of segments are configured into at least one H pattern to form said at least first level; and

Response
Serial No. 09/450,054
Page 5

wherein said at least first level is configured into a hierarchical
succession of H patterns.

Response
Serial No. 09/450,054
Page 6

REMARKS

In the Final Office Action, the Examiner noted that claims 1-11 are pending in the application and that claims 1-11 stand rejected. By this response, claims 1 and 7 are amended to more clearly define the Applicant's invention and not in response to prior art. All other claims continue unamended.

In view of the amendments presented above and the following discussion, the Applicant respectfully submits that none of the claims now pending in the application are anticipated under the provision of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Furthermore, the Applicant also submits that all of these claims now satisfy the requirements of 35 U.S.C. § 112. Thus, the Applicant believes that all of these claims are now in allowable form.

Rejections

A. 35 U.S.C. § 112

The Examiner rejected claims 1-9 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

Claims 1-9

The Examiner rejected claims 1-9 as being indefinite alleging that it is unclear how each level after the first comprises a common point to extend from and also extend from the extremities of the previous order lower level.

In response the Applicant has amended claims 1 and 7 to more particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically the Applicant has amended claims 1 and 7 to claim that the extremities of a previously lower level act as a common point for a plurality of segments of a subsequent level to extend from. As such, the Applicant submits that the basis for the Examiner's rejection of claims 1-9 has been removed, and respectfully requests that the Examiner's rejection of claims 1-9 be withdrawn.

Response
Serial No. 09/450,054
Page 7

Claims 1-9

The Examiner rejected claims 1-9 as being indefinite alleging that it is unclear how what makes up the next order higher level and the previous order lower level.

In response the Applicant has amended claims 1 and 7 to more particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically the Applicant has amended claims 1 and 7 to claim that the extremities of a previously lower level act as a common point for a plurality of segments of a subsequent level to extend from. Claims 1 and 7 further define how each level is comprised of a plurality of segments, each of the segments linearly extending from a common point and having equal lengths, wherein a subsequent order higher level is formed by a plurality of segments, each of the segments having equal lengths and linearly extending from the extremities of a previously order lower level, the extremities of the lower level acting as common points for the segments of the next order higher level to linearly extend from and to form the level. As such, the Applicant submits that the basis for the Examiner's rejection of claims 1-9 has been removed, and respectfully requests that the Examiner's rejection of claims 1-9 be withdrawn.

Having made the changes described above, the Applicant respectfully submits that claims 1-9, as they now stand, are definite and hence fully satisfy the requirements of 35 U.S.C. § 112, second paragraph, and are patentable thereunder.

B. 35 U.S.C. § 102

The Examiner rejected claims 1-2, 4-5, and 10-11 under 35 U.S.C. 102(b) as being anticipated by the Koh et al. patent (United States patent 5,416,861 issued May 16, 1995, hereinafter "Koh"). The rejection is respectfully traversed.

The Examiner alleges that, "Koh et al. disclose a network Fig. 1 for distributing a power signal in an optoelectronic circuit 20 comprising a plurality of

Response
Serial No. 09/450,054
Page 8

electrically conductive pathways forming at least one level, wherein the portions of the conductive pathways are interconnected." The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

The Applicant respectfully submits that Koh does not teach, suggest or disclose each and every element of the Applicant's claimed invention arranged as in the claims. More specifically, Koh discloses an optical waveguide H-tree design for **global clock distribution** on multichip modules (MCM). (See Koh, ABSTRACT). Koh fails, though, to disclose at least the Applicant's invention of claim 1, which specifically recites:

"A network for distributing a power signal in an optoelectronic circuit, said network comprising:

a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths, and wherein the segments of a next order higher level are formed at the extremities of a previous order lower level, the extremities of the previous order lower level functioning as the common point for the formation of the next order higher level;

means for coupling said power signal from a primary input to the common point of the first level; and

terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal." (emphasis added).

There is absolutely no disclosure in Koh for a "network for distributing a power signal in an optoelectronic circuit, said network comprising a plurality of electrically conductive pathways." The "segments 24" cited by the Examiner are

Response
Serial No. 09/450,054
Page 9

not "electrically conductive" as claimed. The Koh reference is simply directed to a different problem than the claimed invention, and the problem is solved in a different manner than claimed here. In contrast to the above quoted claim language, Koh discloses an H-tree configuration for clock distribution (i.e., not power distribution) on MCM substrates using optical rather than electrical interconnection. (See Koh, column 10, lines 57-61.) (emphasis added).

Even further, and maybe of more consequence, there is absolutely no teaching, suggestion, or disclosure in Koh for a network for distributing a power signal in an optoelectronic circuit "wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" as taught by the Applicant's specification and claimed in at least the Applicant's claim 1. More specifically, in support of at least claim 1 the Applicant's in the Specification, specifically recite:

"A new level of the H-tree is formed by coupling the center of the two perpendicular segments of the new level H patterns to the end points of the preceding level H patterns of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway interconnected with one or more other conductive pathways. Since the length of each segment is equal for a respective level, the length of the conductive pathway from the primary input to each terminal node is the same.

In operation, the power distribution tree network utilizes the equal lengths of the conductive pathways of the H-tree network to provide greater bias voltage uniformity to the terminal nodes by eliminating small differences in bias voltage to terminal nodes in different locations of the optoelectronic circuit." (See Specification, page 3, lines 11-23).

It is evident from at least the portion of the Applicant's disclosure presented above, that the Applicant's invention is directed, at least in part, to a network for distributing a power signal in an optoelectronic circuit wherein each of the plurality of segments in each level is of equal length such that a bias voltage for devices connected to the extremities of a final level experience the same bias voltage.

Response
Serial No. 09/450,054
Page 10

In contrast to the Applicant's invention, there is absolutely no teaching, suggestion or disclosure in Koh for a network for distributing a power signal in an optoelectronic circuit wherein each of the plurality of segments in each level is of equal length. The invention of Koh instead is directed to a network for distributing an optical clock signal and not to a network for distributing a power signal in an optoelectronic circuit where each of the plurality of segments in each level is of equal length. As such, the Applicant respectfully submits that the Applicant's invention does have a structural difference over the invention of Koh. Specifically, in the invention of the Applicant, a network for distributing a power signal comprises "a plurality of electrically conductive pathways forming at least a first level wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths". Koh does not teach, suggest or disclose that each of a plurality of segments making up each of the levels all have equal lengths.

In the Final Office Action the Examiner further noted that Koh teaches a that electrical H-tree clock distribution is well-known, however, the Applicant respectfully points out to the Examiner that well-known electrical H-tree clock distribution systems do not teach and do not require that each of the plurality of segments in each level is of equal length. Furthermore, the Examiner noted in the Final Office Action that both electrical signals and optical signals as taught by Koh are power signals. The Applicant respectfully disagrees. The electrical signals and optical signals taught in Koh are clock signals and Koh emphasizes the importance of distributing the clock signal. Koh does not teach, suggest or disclose the distribution of a power signal in an optoelectronic circuit wherein each of the plurality of segments in each level is of equal length such that a bias voltage for devices connected to the extremities of a final level experience the same bias voltage such that the power supplied by terminal nodes to each of a plurality of devices is substantially equal. The power claimed and taught by the Applicant being directed to a biasing voltage. However, there is absolutely no teaching, suggestion or disclosure in Koh for the equal distribution of a bias

Response
Serial No. 09/450,054
Page 11

voltage via a plurality of equal length segments. As such, the Applicant respectfully submits that Koh does not teach, suggest or disclose the invention of the Applicant, at least with respect to claim 1.

Therefore, the Applicant submits that claim 1 is not anticipated by the teachings of Koh and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 10 recites similar relevant features as those recited in claim 1. As such, the Applicant respectfully submits that claim 10 is also not anticipated by the teachings of Koh and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2, 4-5 and 11 depend directly from claims 1 and 10, respectively, and recite additional features therefor. As such and for the exact same reasons set forth above, the Applicant submits that none of these claims is anticipated by the teachings of Koh. Therefore, the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

C. 35 U.S.C. § 103(a)

The Examiner rejected claims 3 and 6-9 under 35 U.S.C. § 103(a) as being unpatentable over Koh as applied to claims 1-2 above, and further in view of Watanabe et al., (U.S. Patent No. 5,309,001). The rejection is respectfully traversed.

Claim 3 and 6

Claims 3 and 6 depend directly from independent claim 1 and recite limitations thereof. The Examiner applied Koh to claims 3 and 6 as described above for the Examiner's rejection of claims 1 and 2. The Examiner alleges that

Response
Serial No. 09/450,054
Page 12

Koh teaches all of the stated limitations except that the pattern of a level is X-shaped. The Applicant respectfully disagrees.

The Examiner correctly concedes that Koh does not teach that the pattern of a level is X-shaped as claimed in claim 3 of the Applicant's invention. However, in addition and as described above, the teachings of Koh do not teach, suggest or describe at least the Applicant's invention at least with regard to claim 1 for "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths." (emphasis added).

Furthermore, the teachings of Watanabe do not teach, suggest, or describe the invention of the Applicant, at least with regard to claim 1. Watanabe teaches a surface electrode on the surface of an LED, wherein the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. (See Watanabe, ABSTRACT). In support of its invention Watanabe teaches:

"At the ends of the sixth-order branches 358a and 358b, there are provided contact portions 359a and 359b for making ohmic contact with the underlying semiconductor layer 351. Meanwhile, the rest of the surface electrode 347 other than the contact portions 359a and 359b is in a state in which a Schottky barrier are yielded on the surface of the semiconductor layer 351." (See Watanabe, col. 16, lines 1-7). (emphasis added).

"Further, since the end portions of the sixth-order (highest-order) branches 358a and 358b and the semiconductor layer 351 are put into successful ohmic contact with each other through the contact portions 359a and 359b while the rest other than the end portions and the semiconductor layer 351 are brought into a state in which the current is suppressed from flowing by the Schottky barrier (i.e. a state in which current will not flow unless a certain high level of voltage is applied), the current can be injected only at the end portions of the surface electrode 351. Accordingly, the light easily goes out of the LED, which leads to further improved external quantum efficiency." (See Watanabe, col. 16, lines 38-50).

Response
Serial No. 09/450,054
Page 13

The structure of the invention of Watanabe, as taught, includes contact portions in the highest-order branches for making ohmic contact with the underlying semiconductor layer. In contrast, the Applicant's invention is directed at least in part to a power distribution network having very different structural limitations. In support of the present invention, the Applicant discloses:

"Terminal nodes are coupled to the endpoints of the last level of the H-tree. In this manner a conductive pathway is formed from the primary input to each terminal node, with portions of each conductive pathway being shared between two or more terminal nodes." (See Specification, page 7, lines 13-16).

"The first level is coupled to the primary input, at the center of the two horizontal segments of the H pattern. The conductive pathways distribute a power signal to terminal nodes 16 (represented by circles and as further indicated in the upper right hand quadrant for a portion of the terminal nodes of FIG. 3) on VLSI chip 20, wherein the distance from the primary input to each terminal node 16 is equal. In this illustrative example, each terminal node 16 represents a VCSEL and its associated driver." (See Specification, page 6, lines 22-29). (emphasis added).

"In operation of the present invention, the effect of voltage drops due to power supply line resistance are reduced when DC power is distributed to the terminal nodes of an optoelectronic circuit, namely the VCSELs in an array of VCSELs of an OE-VLSI chip, with the H-tree power distribution network. Since the lengths of the conductive pathways to each terminal node are equal, there is greater uniformity of the voltage and current provided to each terminal node." (See Specification, page 8, lines 3-8).

It is evident from the Applicant's disclosure, that the Applicant's invention is directed at least in part to a power distribution network for providing uniform power to external devices connected to each terminal node. As such, it is clear that the terminal nodes of the Applicant's invention are not in ohmic contact with an underlying layer. Furthermore, in support of at least claim 1, the Applicant in the Specification specifically recites:

"Each 'H' pattern includes six equal length segments, with two segments in each of two parallel portions and two segments connected

Response
Serial No. 09/450,054
Page 14

perpendicular at the midpoints of the parallel portions to form the H pattern." (See Specification, page 7, lines 3-5).

The Applicant further recites:

"Since the length of each segment is equal for a respective level and the total number of segments to each terminal node is also equal, the length of the conductive pathway from the primary input to each terminal node is the same." (See Specification, page 7, lines 16-19).

It is apparent from the sections of the disclosure presented above that the Applicant's invention is directed at least in part to a power distribution network wherein each of the segments comprising each layer are of equal lengths and the total number of segments connecting each terminal node the primary input are equal. As such, the power provided to each of the plurality of terminal nodes at a last level and subsequently to each of a plurality of connected devices is substantially equal.

The invention of Watanabe is incapable of providing uniform power to devices connected to each terminal node because the surface electrode and the semiconductor layer are in electrical contact with each other at ends of the highest-order branches. The Applicant respectfully submits that at least the structural differences between the highest-order branches of the Applicant's invention and the highest-order branches of the invention of Watanabe make the Applicant's invention patentable over the invention of Watanabe. The Applicant further submits that the structural configuration of the Applicant's highest-order branches are not obvious in view of the invention of Watanabe. The Applicant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Applicant's invention at least with respect to claim 1 and specifically for the structural limitations of the terminal nodes of the Applicant's invention as described above. More specifically, there is absolutely no teaching, suggestion or disclosure in

Response
Serial No. 09/450,054
Page 15

Watanabe for "a plurality of electrically conductive pathways forming at least a first level, wherein each level is comprised of a plurality of segments linearly extending from a common point, each of the segments of respective levels having equal lengths" (emphasis added), as taught by the Applicant's specification and claimed in at least the Applicant's claim 1.

Even further, there is absolutely no teaching, suggestion or disclosure in Watanabe for "terminal nodes coupled at the extremities of a last level for supplying said power signal to a plurality of devices that form at least a portion of said optoelectronic circuit, wherein the number of segments connecting said primary input to each of said terminal nodes is equal such that the power supplied by the terminal nodes to each of the plurality of devices is substantially equal" (emphasis added) as taught by the Applicant's specification and claimed in at least the Applicant's claim 1. Therefore, the Applicant respectfully submits that the Applicant's invention and the invention of Watanabe are directed to two different devices having different structural limitations used for solving different problems. There is absolutely no teaching or suggestion in Watanabe for the Applicant's invention at least with respect to claim 1 and specifically for the structural limitations of the Applicant's invention as described above.

As such, the Applicant respectfully submits that Watanabe does not teach or suggest the Applicant's claim 1. Specifically, the Applicant submits that the structural limitations of at least the Applicant's claim 1 are not taught or suggested by Watanabe.

The Applicant further submits that there is no suggestion or motivation to combine the teachings of Koh and the teachings of Watanabe.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596,

Response
Serial No. 09/450,054
Page 16

1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984);

The Applicant further submits that even if there was a motivation or suggestion to combine the references (which the Applicant believes that there is none), the teachings of Watanabe fail to bridge the substantial gap between the Applicant's invention, and the teachings of Koh.

As such, and at least for the reason that neither Koh or Watanabe alone or in any combination teach suggest, or describe the Applicant's invention with regard to claim 1, the Applicant respectfully submits that dependent claims 3 and 6, which depend directly from independent claim 1, are also not rendered obvious by Koh in view of Watanabe.

Therefore, the Applicant submits that dependent claims 3 and 6 as they now stands, fully satisfies the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

Claims 7-9

The Examiner applied Koh and Watanabe to claims 7 and 9 as described above for the Examiner's rejection of claims 1 and 3 above.

Claim 7 is an independent claim that recites similar relevant features as those recited in claim 1. As described above with regard to the Examiner's rejection of claim 1 and claim 3, the teachings of Koh and Watanabe alone or in

Respon
Serial No. 09/450,054
Page 17

any allowable combination do not teach suggest, or describe the Applicant's invention with regard to claim 1 or claim 3. As such, and at least for the reason that neither Koh or Watanabe alone or in any combination teach suggest, or describe the Applicant's invention with regard to claim 1 and claim 3 for at least the reasons stated above, the Applicant respectfully submits that independent claim 7, which recites similar relevant features as claim 1, and dependent claims 8 and 9, which depend directly from independent claim 7, are also not rendered obvious by Koh in view of Watanabe.

Therefore, the Applicant submits that claim 7 as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Furthermore, dependent claims 8 and 9 depend directly from claim 7 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that none of these claims are obvious with respect to the teachings of Koh and Watanabe, alone or in any allowable combination. Therefore the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicant reserves the right to establish the patentability of each of the claims individually in subsequent prosecution.

Conclusion

Thus the Applicant submits that none of the claims, presently in the application, are anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. § 103. Furthermore, the Applicant also submits that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732)

Response
Serial No. 09/450,054
Page 18

530-9404 x 1131 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



Eamon J. Wall Attorney
Reg. No. 39,414

Dated: 1/15/04
CUSTOMER #26,291
MOSER, PATTERSON & SHERIDAN, LLP
595 Shrewsbury Avenue, Suite 100
Shrewsbury, New Jersey 07702
732-530-9404 - Telephone
732-530-9808 - Facsimile